ARINC 429 IP Core
Datasheet

August 2022

OVERVIEW

ARINC 429 IP Core implements ARINC 429 standard. IP Core contains Rx and Tx processing blocks, Controller Block, Internal Memory and External Memory Interfaces. A429 IP communicates with CPU (Central Processing Unit) and external memory through AXI interface.

IP Core uses AXI interface as internal local bus. AXI interface is 32-bit data bus which has 32-bit addressing, 32-bit read and write channel. IP supports to 32 receive channel number and 16 transmit channel number.

The IP is designed to be compatible with DO-254. ARINC 429 IP is field approved.

FEATURES LIST

i. Supports ARINC 429 Specification

ii. Configurable up to 32 Rx and 16 Tx Channels

iii. Supports 12.5 kbit/s and 100 kbit/s data rates

iv. Contains 32- bit Local Data Bus

v. Contains Individual and Circular buffer area which have 1024 word depth for each channel

vi. Supports single and periodic data transfer

vii. Filter process based on SDI, ESSM and Label section of ARINC 429 Data

viii. Occuring of filter process in FPGA

ix. Communication with CPU and external memory

x. DO-254 compliant

DELIVERABLES

- Encrypted VHDL source code
- ARINC 429 IP Core User Guide
- Optional DO-254 Certification Data Package is available.

LICENSING

Following licensing models are available:

- Encrypted Netlist
- Encrypted RTL
- Encrypted RTL with DO-254 Certification Data Package

Technology Partner

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ARINC 429 IP Core

SUPPORT

With the initial licensing, customers will receive the following services for the first year:

- Half day “IP Core First Time User Training”
- Support during SOI meeting preparations are available with DO-254 Certification Data Package
- IP Core update

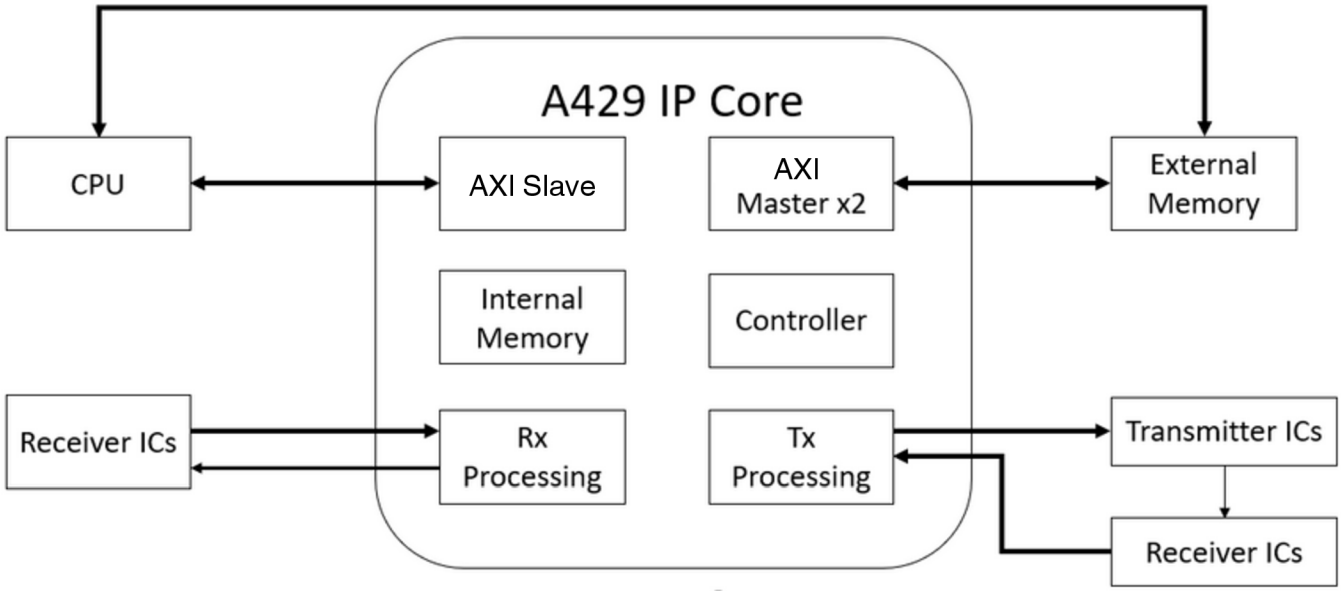
FPGA SYNTHESIS RESULT

The ARINC 429 IP Core can be used in any FPGA family. Encrypted RTL and Encrypted Netlist can be generated according to used any FPGA family. The FPGA resource usage depends on core configuration such as rx and tx channel number.

Family/Device	Configuration	Slice LUTs Needed	Slice Registers Needed	Block RAM Tile Needed	External Memory Needed
Kintex-7/xc7k70tfbv676	3 Rx - 1 Tx	3514	2954	5.5	(2^15)*32-bit
Kintex-7/xc7k70tfbv677	4 Rx - 4 Tx	4817	3925	5.5	(2^15)*32-bit
Kintex-7/xc7k70tfbv678	8 Rx - 4 Tx	6214	4877	7	(2^16)*32-bit
Kintex-7/xc7k70tfbv679	16 Rx - 5 Tx	9041	7183	7	(2^17)*32-bit
Kintex-7/xc7k70tfbv680	16 Rx - 16 Tx	12920	9937	7	(2^17)*32-bit
Kintex-7/xc7k70tfbv681	32 Rx - 16 Tx	18489	13826	8.5	(2^18)*32-bit

Family/Device	Configuration	ALMs Needed	Internal Memory Needed	External Memory Needed
Cyclone V / 5CGXFC7D16F31I7	3 Rx - 1 Tx	2392	178.9 kbit	(2^15)*32-bit
Cyclone V / 5CGXFC7D16F31I7	4 Rx - 4 Tx	3297	179.1 kbit	(2^15)*32-bit
Cyclone V / 5CGXFC7D16F31I7	8 Rx - 4 Tx	4104	179.7 kbit	(2^16)*32-bit
Cyclone V / 5CGXFC7D16F31I7	16 Rx - 5 Tx	5959	181.2 kbit	(2^17)*32-bit
Cyclone V / 5CGXFC7D16F31I7	16 Rx - 16 Tx	8682	181.9 kbit	(2^17)*32-bit
Cyclone V / 5CGXFC7D16F31I7	32 Rx - 16 Tx	12086	184.4 kbit	(2^18)*32-bit

BLOCK DIAGRAM



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