ELECTRA IC
Design & Verification

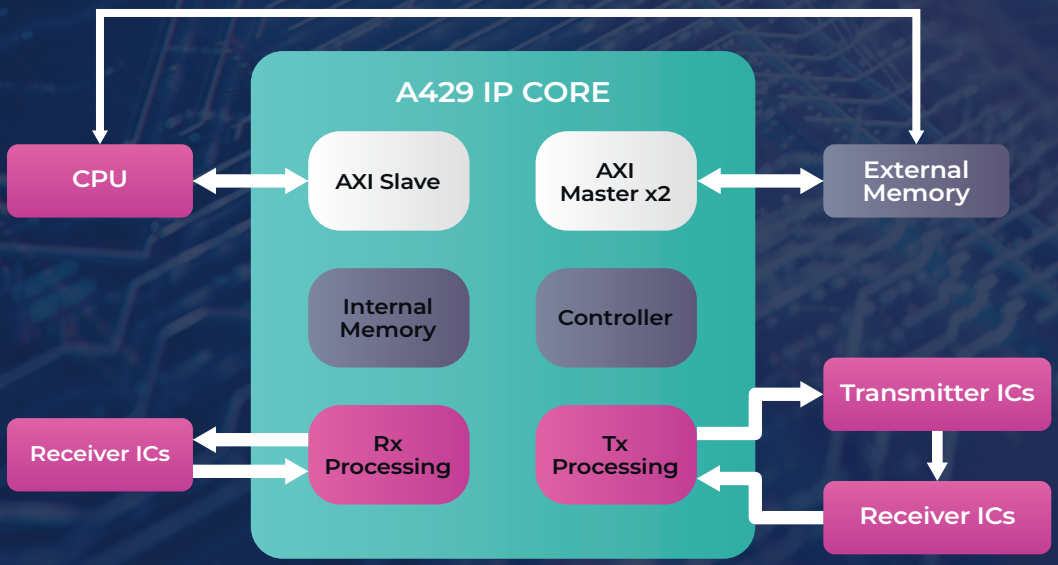
ARINC 429 IP

ARINC 429 IP is an IP Core which implements ARINC 429 standard and IP contains Rx and Tx Processing Blocks, Controller Block, Internal Memory and External Memory Interfaces. A429 IP communicates with CPU (Central Processing Unit) and external memory through AXI interface.

SPECS

- Supports ARINC 429 Specification
- Configurable up to 32 Rx and 16 Tx Channels
- Supports 12.5 kbit/s and 100kbit/s data rates
- Contains 32-bit local data bus
- Contains Individual and Circular buffer area which have 1024 word depth for each channel
- Supports single and periodic data transfer
- Filter mechanism based on SDI, ESSM, Label of ARINC 429 data
- Occuring of filter process in FPGA
- Communication with CPU and external memory
- Field Approved
- DO-254 compliant

BLOCK DIAGRAM



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