ELECTRA IC
Design & Verification

ARINC664
END SYSTEM IP
EIP-20E24

ARINC664 End System IP is an IP Core that implements ARINC664 part 7 and provides interface between aircraft LRUs and ARINC664 network. As an implementation of End System, IP sends the user's messages of different sizes and different time constraints to their destination with a predictable delay. Since the IP core uses the Ethernet interface when connecting to the network, it takes full advantage of the physical layer functions that Ethernet offers. Thanks to the AXI4 interface provided with IP Core, adaptation can be made between any protocol and ARINC664.

FUNCTIONAL SPECS

- Supports 32 VLs
- Adjustable BAG values (1ms to 128ms, 125us to 32ms)
- Supports 64 Byte as Lmin and 1471 Byte as Lmax
- Redundancy enable/disable capability
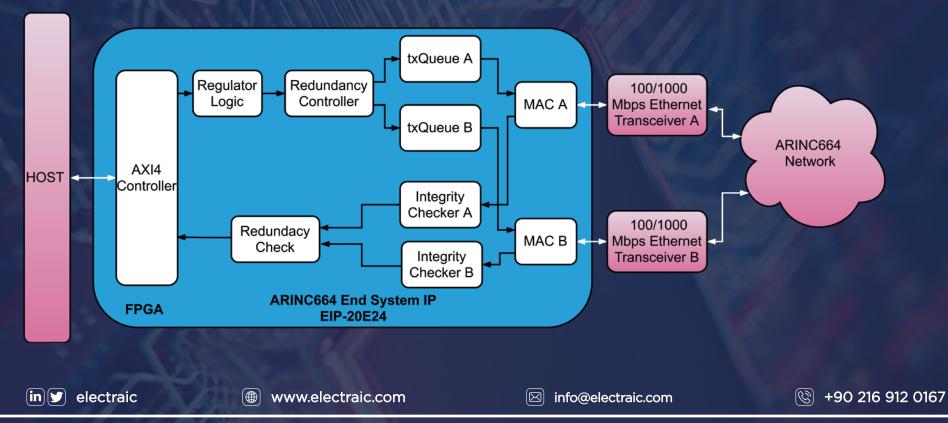- Integrity Checking enable/disable capability
- Outputs error statistic

INTERFACE SPECS

- AXI4 interface for host communication
- Two ARINC664 Ethernet interfaces
- End System configuration through AXI4 interface
- 100 Mbps/1000 Mbps Ethernet speed

BLOCK DIAGRAM

HOST

AXI4 Controller

Regulator Logic

Redundancy Controller

txQueue A

txQueue B

MAC A

100/1000 Mbps Ethernet Transceiver A

Integrity Checker A

Redundacy Check

Integrity Checker B

MAC B

100/1000 Mbps Ethernet Transceiver B

ARINC664 Network

FPGA

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