

**ARINC664
SWITCH IP
EIP-20S24**



ARINC664 Switch IP implements ARINC664 part 7 and provides switching functionality within the ARINC664 network. As an implementation of ARINC664 Switch, IP switches/routes messages of different sizes and different time constraints to their destination with a predictable delay. Two level of priority can be applied to the VLs during configuration of the device. Thus, switch can arrange the data queues according to these priorities. Thanks to the AXI4 interface provided with IP Core, error statistics can be fetched to a desired logic and data injection to the network can be accomplished if desired.



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FUNCTIONAL SPECS

- Supports 128 VLs
- Adjustable BAC values
- Supports 64 Byte as Lmin and 1471 Byte as Lmax
- Adjustable message priority (two classes)
- Multicasting ability
- Outputs error statistic

INTERFACE SPECS

- AXI4 interface for host communication
- Eight ARINC664 Ethernet interfaces
- End Switch configuration through AXI4 interface
- 100 Mbps/1000 Mbps Ethernet

BLOCK DIAGRAM

