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ELECTRA IC
Design & Verification

Advanced Verification Techniques Training

4 Weeks

electraic www.electraic.com trainings@electraic.com +90 216 912 0167

Training Course

Week	Program
1	SystemVerilog Training
2	UVM Training and Practical Application
3	Setting Up A Verification Environment Using VIP
4	Use of Documentation in Verification Evaluation

Advanced Verification Techniques Training offers a compact training program to meet the requirements of hardware design engineers. Our training is designed to enable designers to develop their capabilities by leveraging SystemVerilog features for their overall design and validation requirements, including RTL Coding, Assertions and Testcases.
In addition, designers will have the opportunity to install the UVM (Universal Verification Methodology) environment, a standard functional verification methodology developed for SystemVerilog, from scratch.
They will verify the design they have achieved in Digital Design and VHDL Training using VIP.

Learning Outcomes

Bus-Functional Modeling
Basic Data Types
Interfaces
The SVA Language
Properties and Assertions
Clocking Blocks
Randomization
Coverage
Arrays and Queues
Classes for Transactions
Class Members and Copying
Virtual Interfaces
Extending Classes for Stimulus
TLM and Channels
Component Hierarchy
Monitors and Checkers
Functional Coverage
Factory and Configuration
Agent Architecture
Objections
Sequences
Layered Sequences
Events and Barriers
UVM Register Layer