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BY



 **ELECTRA IC**
Design & Verification

Digital Design and VHDL Training

 **4 Weeks**



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Training Course

Week	Program
1	Introduction to Digital Design and VHDL Training
2	RTL Design with VHDL
3	RTL Verification with VHDL
4	RTL Verification and Tests on FPGA card Evaluation

Digital Design and VHDL Training is a comprehensive training program prepared for those who are interested in digital design, either be a new graduate or an engineer who wants to develop his/her skills in this field. Thanks to this intensive training program and the hands-on exercises; our trainees learn digital design techniques in a very short period of time, which will otherwise take months to learn.

Learning Outcomes

Digital Design Basics
Synchronous Design
Digital Design Technologies
Design Practices
Common Functions
Arithmetic Structures
Outside the Synchronous World
Finite State Machines
IP Blocks
FPGA Design Flow
Design Entities
Processes
Synthesising Combinational Logic

Types
Synthesis of Arithmetic
Synthesising Sequential Logic
FSM Synthesis
Memories
Basic TEXTIO
Managing Hierarchical Designs
Parameterised Design Entities
Procedural Testbenches
Text-File-Based Testbenches
Gate Level Simulation



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