

EAVS ElectraIC Advanced Verification Suite

Accelerate Your Verification with ElectraIC Advanced Verification Suite!

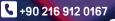
Tired of lengthy setup times for your verification environments? Introducing our Configurable UVM Verification Environment, designed to simplify and speed up the verification process for engineers. Whether you're working with third-party VIPs or custom-designed VIPs, this environment is ready to support your verification needs.

KEY FEATURES

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- Plug & Play Flexibility: Easily integrate any VIP into our environment, eliminating the need for complex setups.
- **Configurable & Scalable:** Adapt the environment to fit your project, whether you're verifying a simple block or a complex system.
- **RISC-V Ready:** Includes Google-DV RISC-V Instruction Set Simulator for seamless verification of any RISC-V cores.
- **Time & Effort Savings:** Focus on your tests and verification, not on the environment setup. Our solution significantly reduces the time and effort required to get your verification environment up and running.

Ready to make your verification process more efficient? Contact us today!



EAVS

BLOCK DIAGRAM

| SoC/RISC-V VM Environmen | nt | | | | ISS Verification Environment | Firm |
|----------------------------------|----------------------------|-------------------------------------|-----------------------------------|--------------------------------|------------------------------|------|
| Base Agent | SPI Agent | Custom UVC Agent | UART Agent | I2C Agent | Coverage Collector | Com |
| Ethernet Agent | DDR4 Agent | PCIe Agent | Wishbone Agent | AXI-4 Agent | object | |
| Base Coverage Collector | Collector C | Custom UVC Coverage Collector | overage California | I2C Coverage Collector | risc-v asm generator | |
| Ethemet Coverage Collector | DDR4 Coverage Collector | PCle Coverage Collector | Wishbone Coverage Collector | AXI-4 Coverage Collector | | Boot |
| Base Scoreboard | SPI Scoreboard | Custom UVC Scoreboard | UART Scoreboard | I2C Scoreboard | | |
| Ethernet Scoreboard | DDR4 Scoreboard | PCIe Scoreboard | Wishbone Scoreboard | AXI-4 Scoreboard | | |
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OVERVIEW

EAVS is a plug and play verification environment based on SystemVerilog and UVM. EAVS offers an environment to meet RISC-V/ARM based design verification needs in sectors such as automotive, defense, mobile, etc. It includes an Instruction Set Simulator environment for processors and a VIP-supported interface verification environment for the most widely used interfaces in the specified sectors such as UART, I2C, SPI, PCIe, Ethernet, AXI Standards, DDR2/3/4. It also provides the necessary infrastructure for testing accelerator structures.

FEATURE LIST

- SystemVerilog/UVM Based Verification Environment
- Instruction Set Simulator Based RISC-V IP Verification support
- Optional ISS integration support for third-party solution providers
- Google DV Based Random Instruction Set Generator support
- Compile and Simulation Scripts Infrastructure for Siemens Questa Prime, Synopsys VCS and CDS Xcellium
- Configuration Interface to customize the verification environment at upper level
- Ready to use Verification Environment with major EDA Vendor Verification IPs
- Ability to connect easily third-party/custom Verification IPs and agents

🐱 info@electraic.com

