ELECTRA IC
Design & Verification

High Reliability Mission Critical FPGA and SoC Design

3 Days

Program Overview

FPGA's and heterogeneous SoC's are used in an increasing number of mission critical or high reliably applications. These applications span a diverse range from industrial, medical and scientific to defence, transportation and even space. For these devices to safely and reliably operate in an often-harsh environment, a more rigorous design approach is required. This design approach should introduce both stricter engineering governance in the design process and design mitigation techniques.

As such, designing these solutions requires the designer to not only understand what techniques can be used at the logic level but also, the wider systematic, regulatory and environmental isues.

This course will therefore present the environmental challenges and what they mean to the logic designer. Along with introducing high level concepts such as SIL level, Reliability and Mean Time to Failure. Attendees will also gain an understanding of the importance of engineering governance.

Who should attend?

FPGA Designers ve Digital IC Design Engineers.

Pre-requisites?

It is expected that the atendee is an experienced FPGA designer and has familiarity with electronics and system engineering concepts.

What will you learn?

The focus of this course is the development of techniques which can be used in programmable logic including Clocking & Reset strategy, Triple Modular Redundancy, IO Planning, Safe State Machines and Counters, Error Correcting Codes, Single Event Effect Mitigation along with Verification strategies and metrics, formal equivalence checking, Synthesis strategies and several other advanced techniques.

Training Materials

Hardcopy and softcopy of the training materials will be provided.

Structure and Content

1. How the environment impacts our designs

- Temperature, Shock & Vibration, EMC and Radiation

2. Programmatic / System level considerations

- Different Standards 61508 / DO254 / ISO26262
- The design life cycles
- Engineering Governance
- What is reliability & what does MTBF mean & what impacts the MTBF
- Requirement capture & progressive verification
- Architectural design & interdependency of faults between SW and HW
- Common cause failures & failure mode & redundancy
- Worse case analysis

3. FPGA Design Considerations

- FPGA Development overview & Supporting Documentation
- Device Selection – OTP, FLASH, SRAM
- Coding Style & Certified tools
- Failure modes
- Self-Test and Diagnostics
- Clocks and Resets & IO planning & JTAG / Boundary Scan
- Safer state machines & counters
- Error correcting codes communications and memories
- Triple modular redundancy local, fine grain and global
- Functional separation within the device, Isolation flow
- Single event efects and configuration corruption
- Verification & verification metrics
- Fault injection
- Timing closure
- Advanced Features e.g. XADC, SysMon