ELECTRA IC
Design & Verification

IC Design Flow Essentials

3 Days

Program Overview

• Targets 2 critical areas of IC design which allow trainee to further understand of IC design flow with industry standard IC design software.

• Modules include extensive hands on lab work to ensure trainees are able to use the tools effectively and efficiently.

Technology Focus

Covering 2 Critical Areas of IC Design

• Logic Implementation - Synthesis and DFT

• Physical Implementation - Place and Route

In this training, objectives are;

• To equip trainee with knowledge of industry standard Electronic-Design-Automation (EDA) Software

• To enhance design-problem solving skill

• To increase knowledge in IC design flow

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Pre-requisites

Basic knowledge in digital logic and semiconductor physics.

Who should attend?

- This training is designed for engineers willing to improve their IC design flow knowledge.
- The training covers front-end design and back-end design flow steps.
- Participants will have a good understanding of IC design flow after completion of this training.

What will you learn?

- All the IC design steps of front-end and back-end flow will be covered in this training.
- Logic synthesis and implementation section will cover standard cell design, timing constraints, design optimization, and static timing analysis and power analysis.
- Design for Testability section will cover scan and IDDQ testing.
- Physical implementation section will cover floorplanning, cell placement, clock tree synthesis, routing, physical verification and design output.
- Labs/hands on is not included in 3-days IC Design Flow Essentials but included in 5-days IC Design Flow Hands-on course.

Training Materials

Hardcopy and softcopy of the training materials will be provided.

Structure and Content

1. Introduction to VLSI SoC Design flow

- Descriptions
- Goal

2. Logic Synthesis and Implementation

- Introduction to standard cell design
- Design constraint
- Design optimization
- Timing and Power Analysis

3. Design For Testability

- IC testing overview
- Fault modeling
- Scan Test
- IDDQ

4. Physical Implementation

- Design planning
- Cell Placement
- Clock tree building
- Routing
- Physical verification
- Design output