ELECTRA IC
Design & Verification

# IC Design Flow Hands-on

5 Days

## Program Overview

• Targets 2 critical areas of IC design which allow trainee to further understand of IC design flow with industry standard IC design software.

• Modules include extensive hands on lab work to ensure trainees are able to use the tools effectively and efficiently.

## Technology Focus

Covering 2 Critical Areas of IC Design

• Logic Implementation - Synthesis and DFT

• Physical Implementation - Place and Route

In this training, objectives are;

• To equip trainee with knowledge of industry standard Electronic-Design-Automation (EDA) Software

• To enhance design-problem solving skills

• To increase knowledge in IC design flow

## Pre-requisites

Basic knowledge in digital logic and semiconductor physics.

## Who should attend?

- This training is designed for engineers willing to improve their IC design flow knowledge.
- The training covers front-end design and back-end design flow steps.
- Participants will have a good understanding of IC design flow after completion of this training.

electraic www.electraic.com trainings@electraic.com +90 312 429 0067

## What will you learn?

- All the IC design steps of front-end and back-end flow will be covered in this training.
- Logic synthesis and implementation section will cover standard cell design, timing constraints, design optimization, and static timing analysis and power analysis.
- Design for Testability section will cover scan and IDDQ testing.
- Physical implementation section will cover floorplanning, cell placement, clock tree synthesis, routing, physical verification and design output.
- Labs/hands on is not included in 3-days IC Design Flow Essentials but included in 5-days IC Design Flow Hands-on course.

## Training Materials

Hardcopy and softcopy of the training materials will be provided.

## Structure and Content

1. **Introduction to VLSI SoC Design flow**
   - Descriptions
   - Goal

2. **Logic Synthesis and Implementation with Design Compiler**
   - Intro to Synthesis
   - Setting up and saving designs
   - Design & library objects
   - Design constraints
   - Synthesis & Optimization technique
   - Timing analysis
   - Post-synthesis output

3. **Design For Testability with DFT Compiler**
   - Test protocols
   - DFT for clocks & reset
   - Top down scan insertion
   - Exporting design files
   - ATPG

4. **Physical Implementation with IC Compiler**
   - Data setup & basic flow
   - Design planning
   - Placement
   - Clock tree synthesis
   - Routing
   - Chip finishing

**Tools to be used during the course**

- Redhat Linux Enterprise 6.6 or Centos 6.6 and above
- Synopsys EDA

1. **Logic Implementation**
   - DC Ultra
   - DesignWare Library
   - Design Vision
   - HDL Compiler
   - DFT Compiler
   - TetraMax
   - Library Compiler

2. **Physical Implementation**
   - IC Compiler
   - StarRC
   - IC Validator
   - Milkyway