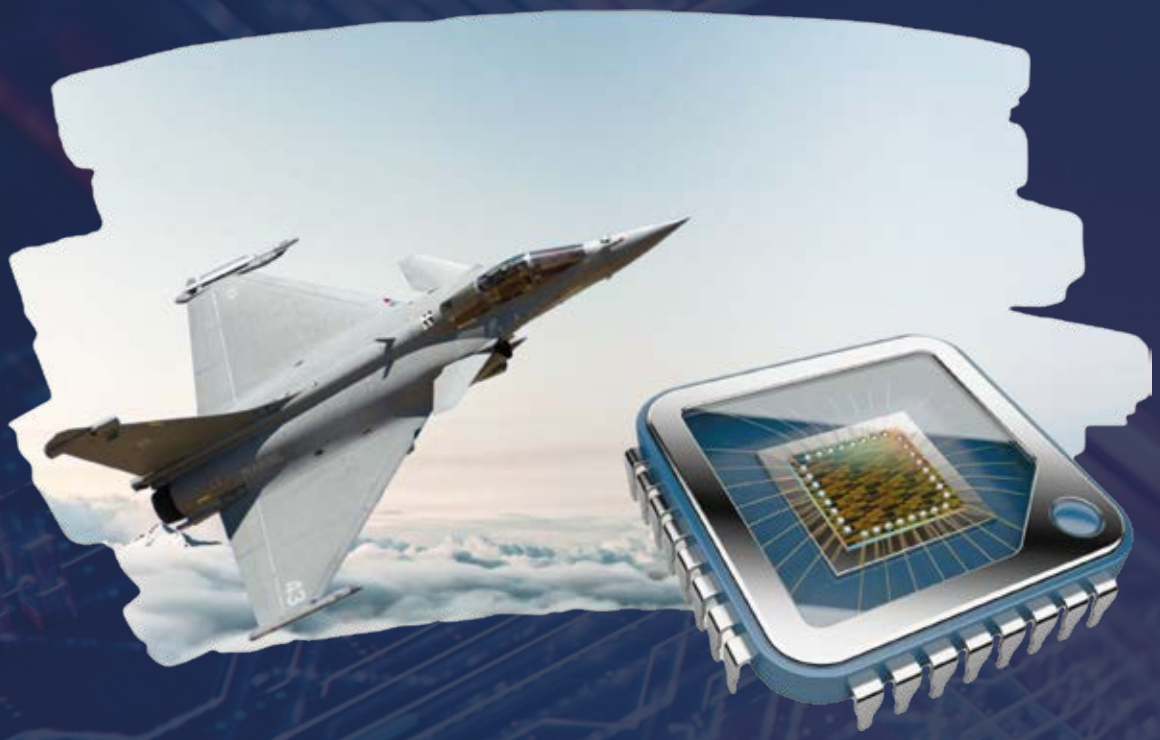
ELECTRA IC
Design & Verification

MIL-STD-1553 IP



MIL-STD-1553 IP is an IP Core which implements MIL-STD- 1553B standard and provides single or multi-functional interface between host processor and MIL-STD-1553 bus transceiver.
MIL-STD-1553 IP can function simultaneously at the same time as Bus Controller (BC), two separate Remote Terminal (RT) and Bus Monitor (BM).

electraic www.electraic.com info@electraic.com +90 216 912 0167

COMMON SPECS

- 64K bytes internal static RAM with RAM Error Detection/Correction option
- 16-bit time tag counters and clock sources for all terminals
- 64-Word Interrupt Log Buffer
- Built-in and optional self-test for protocol logic, digital signal paths and internal RAM
- Programmable 50/100 MHz Clock Frequency

BUS CONTROLLER SPECS

- Fully programmable Bus Controller
- Bus Controller has 32-bit time count options
- Programmable Status Set
- Message Format Check
- 16 Condition Code for all opcode
- 64-Word General Purpose Queue for external BC Host
- Programmable Inter-Message Gap Time (resolution 1us)
- Programmable Message Timeout

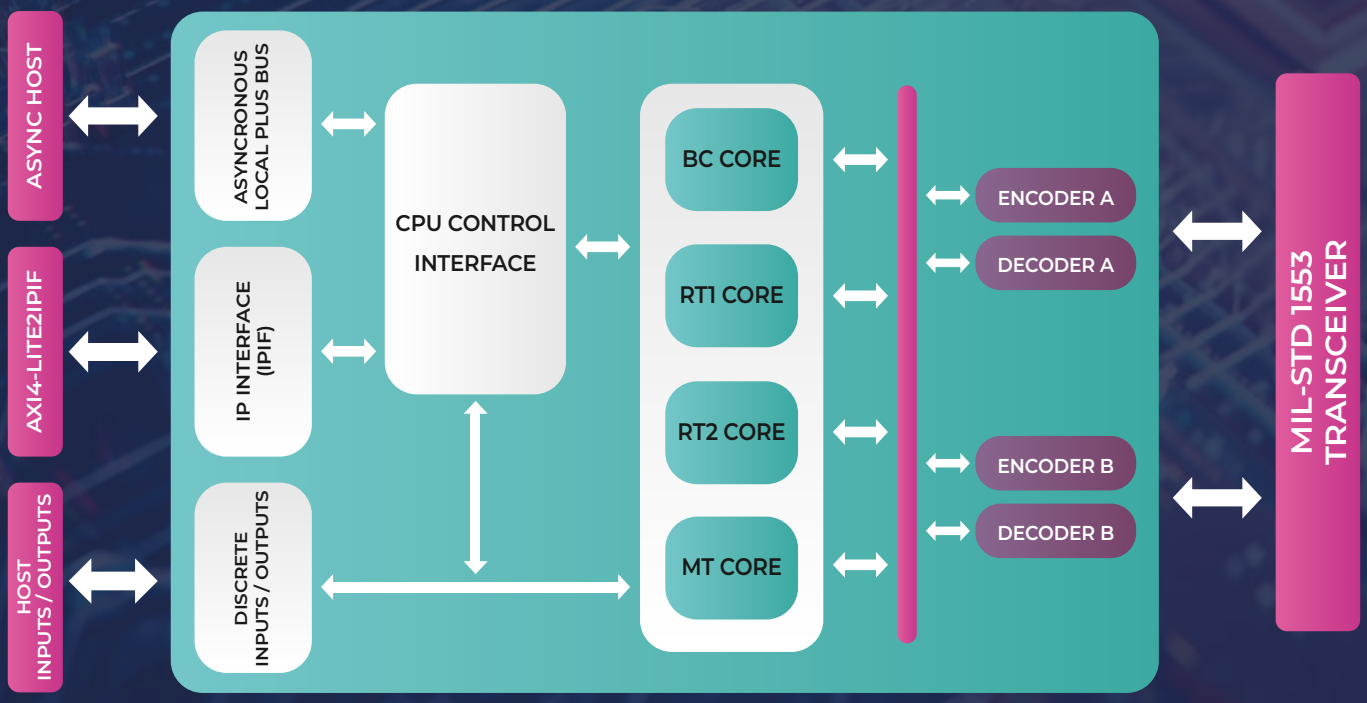
REMOTE TERMINAL SPECS

- Two independent Terminal Core
- Programmable different buffer mode for all Subaddress
- Subaddress based illegal command declaration
- Optional temporary buffer

BUS MONITOR SPECS

- Basic Bus Monitor (BBM) records commands and data separately, with 16-bit or 48-bit time tagging
- Optional support function for IRIG-106 data packets, including full packet headers and trailers
- Bus Monitor has 32 and 48-bit time count options
- Message Filter Table

BLOCK DIAGRAM



electraic www.electraic.com info@electraic.com +90 216 912 0167