MIL-STD-1553B IP Core

Datasheet

June 2020

OVERVIEW

MIL-STD-1553B IP Core implements MIL-STD- 1553B standard and provides single or multi-functional interface between host processor and MIL-STD-1553 bus transceiver. DO-254 compliant MIL-STD-1553B IP core can function as Bus Controller (BC), two separate Remote Terminals (RT) and Bus Monitor (BM), simultaneously.

The MIL-STD-1553B IP Core uses standard AXI4 – Lite interfaces to ease integration or Asynchronous Host Interface (Local Plus Bus). Its configuration and status registers are accessible via a 16-bit-wide IPIF (IP Interface) bus. Auto Enable configuration is supported via EEPROM.

The MIL-STD-1553B IP Core is available in synthesizable RTL (VHDL) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

DELIVERABLES

- Encrypted Netlist
- Synthesis Scripts
- Comprehensive Documentation
- Device Driver for Xilinx SDK (Bare-metal)
- Optional SystemVerilog/UVM Advanced Verification Environment delivery. Needs extra MIL-STD-1553B VIP license.
- Optional DO-254 Certification Data Package is available.

MAINTENANCE & SUPPORT

With the initial licensing, customers will receive the following services for the first year:

- Half day “IP Core First Time User Training”
- E-mail and telephone technical support
- 2 days on-site support (only in Türkiye)
- Additional on-site support available if requested
- Support during SOI meeting preparations are available with DO-254 Certification Data Package
- IP Core updates

Above services can be received after the first year by renewing the maintenance agreement.

LICENSING

Following licensing models are available:

- Encrypted Netlist
- Encrypted RTL
- Encrypted RTL/Netlist with IP Core Verification Environment
- Encrypted RTL with DO-254 Certification Data Package

Following licensing modes of the IP Core is available. Per part prices will differ depending on the below modes.

- 2RT/BC/BM
- 1RT
- 1 BC
- 1BM

FEATURES LIST

a. COMMON SPECS

i. 64K bytes internal static ram with RAM Error Detection/Correction option

ii. 16-bit time tag counters and clock sources for all terminals

iii. 64-WORD Interrupt Log Buffer

iv. Built-in and optional self-test for protocol logic, digital signal paths and internal RAM

v. Programmable 50/100 MHz Clock Frequency

vi. Complete reference designs available for Xilinx

vii. Total RTL verification test cases performed: 893

viii. Total FPGA verification test cases performed: 844

b. BUS CONTROLLER SPECS

i. Fully programmable Bus Controller

ii. Bus Controller has 32-bit time count options

iii. Programmable Status Set

iv. Message Format Check

v. 16 Condition Code for all opcodes

vi. 64-Word General Purpose Queue for External BC Host

vii. Programmable Inter-Message Gap Time (resolution 1us)

viii. Programmable Message Timeout

ix. Certified per

- SAE AS4113 Validation Test Plan for the Digital Time Division Command/ Response Multiplex Data Bus Bus Controllers
- SAE AS4114 Production Test Plan For The Digital Time Division Command/ Response Multiplex Data Bus Bus Controllers

c. REMOTE TERMINAL SPECS

i. Two Independent Terminal Cores

ii. Programmable different buffer mode for all sub-address

iii. Sub-address based illegal command declaration

iv. Optional temporary buffer

v. Certified per

- SAE AS4111 Validation Test Plan for the Digital Time Division Command/ Response Multiplex Data Bus Remote Terminals
- SAE AS4112 Production Test Plan For The Digital Time Division Command/ Response Multiplex Data Bus Remote Terminals

d. BUS MONITOR SPECS

i. Basic Bus Monitor (BBM) records commands and data separately, with 16-bit or 48-bit time tagging

ii. Optional support function for IRIG-106 data packets including full packet headers and trailers

iii. Bus Monitor has 13-bit and 48-bit time count options

iv. Message Filter Table

v. Certified per

- SAE AS4116 Test Plan for the DigitalTime Division Command/Response Multiplex Data Bus Bus Monitors

MIL-STD-1553B IP Core

ORDERING

MIL-STD-1553 IP Core can be ordered in the following quantities. Pricing differs according to the order quantity. Minimum order quantity is 20.

Order Quantity
20 - 99
100 - 499
500+

RELATED PRODUCTS

MIL-STD-1553B IP Core is compatible with MIL- STD-1553 Board and will be included in this board when ordered.
MIL-STD-1553B VIP license is included with the Verification Environment or can be purchased separately.

FPGA SYNTHESIS RESULT

The MIL-STD-1553B IP Core can be mapped to any FPGA device (provided sufficient silicon resources are available). The FPGA resources requirements depend on the core configuration.

Family/Device	Configuration	LUT	FF	BRAMs
Zynq/Xc7z010	Only RT 1	6675	3969	28.00
Zynq/Xc7z010	RT1 and RT2	10021	5691	28.00
Zynq/Xc7z010	Only BC	5531	3286	28.00
Zynq/Xc7z010	Only BM	7202	2572	28.00
Zynq/Xc7z010	RT1, BC, BM	12949	6550	28.00
Zynq/Xc7z020	RT1, RT2, BC, BM	16528	8279	28.00

Family	Configuration	Fabic 4LUT	Fabric DFF	4LUT/DFF	uSRAM/ LSRAM
MPF100T	Only RT 1	12007	5726	2244/2244	19/56
MPF100T	RT1 and RT2	16466	7478	2244/2244	19/56
MPF100T	Only BC	11894	3990	2244/2244	19/56
MPF100T	Only BM	12680	4870	2244/2244	19/56
MPF100T	RT1, BC, BM	21839	8712	2244/2244	19/56
MPF100T	RT1, RT2, BC, BM	17412	7700	2244/2244	19/56

BLOCK DIAGRAM