ELECTRA IC
Design & Verification

PRACH IP Suite

Optimize your 5G NR O-RAN Split 7.2X design with EIC cutting-edge PRACH Design and Verification Suite. This comprehensive suite includes an end-to-end MATLAB model, RTL implementation of the MATLAB model, and a robust verification environment for bit-exact simulation and testing. Ensure seamless integration and accelerate your development process with EIC 5G NR O-RAN compatible solution.

Overview:

- **Comprehensive Support:** All PRACH formats and configuration indexes described in 3GPP 38.211 are fully supported.
- **Versatile Sequences:** Length-139 and length-839 sequences are included.
- **Frequency Multiplexing:** Capable of decoding up to 8 frequencies multiplexed PRACHs.
- **Flexible Subcarrier Spacing:** Supports both 15 and 30 kHz PRACH subcarrier spacing for short formats.

Specifications:

Frequency Range	FR1
Duplex Mode	TDD
Numerology	1
Maximum Frequency Multiplexing	8
Supported Input Sampling Rates	30,72; 61, 44; 122,8 MSPS
PRACH Format Support	All formats
PRACH Configuration Index Support	All Indexes
PRACH Length Support	139, 839

PRACH MATLAB Model:

- **O-RAN Compatibility:** Input stimuli generation and C-Plane Section Type: 3 message generation for each PRACH occasion.
- **Configurable Input:** Option to constrain the number of frames and resource blocks.
- **Advanced Signal Processing:** Three signal processing chains implemented:
  1. *Full frequency-domain PRACH extraction in double data format for golden reference.*
  2. *Hybrid frequency and time-domain PRACH extraction in double data format using MATLAB's high-level functions for proof of concept.*
  3. *Hybrid frequency and time-domain PRACH extraction in fixed-point data format for RTL implementation.*
- **Precision PDP Calculation:** Performed at the end of each processing chain.
- **Configurable Bit Reduction:** Allows adjustment of bit reduction amounts at each module's output.
- **Data Dumping:** Possible after each module.

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PRACH

PRACH RTL Design:

- **Direct Implementation:** RTL implementation of the MATLAB model's fixed-point signal processing chain.
- **Extensive Frequency Resource Extraction:** Capable of extracting up to 8 PRACH frequency resources.
- **Detailed Information:** Provides CC ID, Section ID, and RU Port ID information.
- **Flexible Decimation:** Supports 1 to 96x decimation.
- **Robust FFT Support:** Handles 256 to 8192 point FFT after decimation.
- **Industry Standard Interface:** Utilizes AXI4-Stream interface.

PRACH RTL Test Environment:

- **AXI4-Stream IQ Data Driver:** Takes input stimuli generated by the MATLAB model and feeds them into the RTL signal processing chain.
- **C-Plane Section Type:** 3 Message Driver: Processes C-Plane messages generated by the MATLAB model and feeds them into the RTL signal processing chain.
- **MATLAB Model-Based Reference:** The PRACH Design and Verification Suite uses the MATLAB model as a reference, allowing for the comparison of outputs from sub-blocks with MATLAB references. This feature simplifies the debugging process and enhances verification accuracy.
- **Extensive Test Scenario Support:** Provides RTL verification scenarios for all PRACH formats and indexes.

BLOCK DIAGRAM