# SmartDV™

## Proven and Trusted Smart Design and Verification Solutions™

### VERIFICATION

Industry's Most Comprehensive Portfolio

Full Design Cycle Support: Verification IP, Formal, Emulation, Post-Silicon

New! RISC-V CPU Verification Platform

### SUPPORT

Rapid, On-Demand Creation and Customization of Design IP and Verification IP

Verification and Design Services
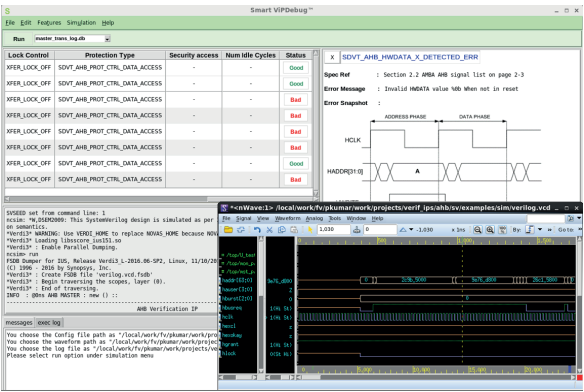
### DESIGN

All Protocols Supported

Rapid, On-Demand Customization

**Product Brochure**

# SmartDV… the Smart Choice for Design and Verification IP Solutions

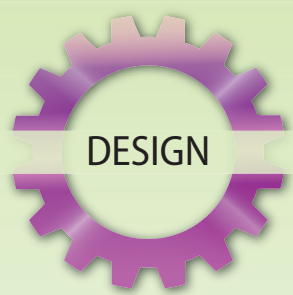## Comprehensive Verification and Design IP Solutions

- **New from SmartDV** – **RISC-V CPU Verification Platform** provides a push-button approach to CPU verification and supports all RISC-V ISAs.

- **Verification IP** for mobile, networking, SoC, automotive, serial bus, storage, video, memory, mil-aero and other protocols.

- **Accelerators for Emulation and FPGA** via SimXL™ Synthesizable Transactors accelerate emulation and FPGA prototyping and offer a seamless transition from simulation.

- **Formal IP** for assertion-based formal verification compatible with all popular formal verification and simulation environments.

- **Design IP** supports all industry standard protocols and interfaces and can be rapidly customized on-demand.

- **Post-Silicon ViP** supports verification of new silicon via FPGA platform and Linux Perl driver.

- **SmartVIPDebug™** provides rapid analysis and debug via advanced waveform and tabulated transaction views.

- **Support and Services** for rapid customization/creation of ViP and Design IP and design and verification project services.

## SmartDV Solutions Span the Design Cycle



### DESIGN

- Support for All Industry Protocols
- Rapid Customization of Design IP to Meet Specific Customer Requirements
- Design IP Developed by Experienced ASIC Engineering Team

### VERIFICATION

- Support for All Industry Protocols
- Compatible With All Verification Languages, Platforms and Methodologies
- Seamless Verification Across The Entire Design Cycle
  - Verification IP for Simulation
  - Synthesizable Transactors – SimXL for Accelerating Emulation and FPGA Prototyping*
  - Formal IP to Assertion-Based Formal Verification
  - Post-Silicon IP

\* Support for Palladium®, sēmu™, Veloce®, and ZeBu® Emulation Platforms and HAPS®, and HyperSilicon FPGA Prototyping Platforms

### SUPPORT

- Fast Turnaround, On-Demand Customization or Creation of Verification and Design IP
- Unmatched Technical Support Team with Years of Experience in ASIC Design and Verification
- On-Demand Services for Verification and Design Projects



## SmartViPDebug™ Speeds and Simplifies Debugging

- Visual debug and tabulated transaction views provide rapid pinpointing of issues
- In-sync debug between waveform and tabulated views

- All protocols supported – in-depth knowledge of the detailed protocol specification not required
- Compatible with all SmartDV ViPs

## The World's Leading Design and Verification Teams Rely on SmartDV's Proven and Trusted Design and Verification IP Solutions

- Most comprehensive and up-to-date portfolio of proven Verification IP and Design IP
- RISC-V CPU verification platform delivers push-button support for CPU verification and supports all RISC-V ISAs

- SmartDV verification products cover the design cycle from simulation, formal verification, emulation and FPGA prototyping and post-silicon verification
- Proprietary SmartCompiler™ delivers rapid creation and customization of Verification and Design IP

# The World's Largest Portfolio of Verification and Design IP

## A Sampling of SmartDV's Extensive VIP and Design IP

| Verification IP Protocol | Verification IP | SimXL * | Assertion IP | Post-Silicon VIP |
|---|:---:|:---:|:---:|:---:|
| Advanced VCI | ✓ | | | |
| AMBA ACE | ✓ | | ✓ | |
| AMBA ACE5 | ✓ | | ✓ | |
| AMBA ACE5-Lite | ✓ | | ✓ | |
| AMBA ACE-Lite | ✓ | | ✓ | |
| AMBA AHB | ✓ | ✓ | ✓ | |
| AMBA AHB5 | ✓ | ✓ | ✓ | |
| AMBA AHB5 Bus | ✓ | ✓ | ✓ | |
| AMBA AHB Bus | ✓ | ✓ | ✓ | |
| AMBA AHB-Lite | ✓ | ✓ | ✓ | |
| AMBA AHB-Lite Bus | ✓ | ✓ | ✓ | |
| AMBA APB3 | ✓ | ✓ | ✓ | |
| AMBA APB4 | | | | |

| Design IP Protocol |
|---|
| 10/100/1000M MAC Controller |
| 10G MAC Controller |
| 1G TSN MAC Controller |
| AC97 Controller |
| AVSBUS Master |
| AVSBUS Slave |
| CAN Controller |
| eMMC Device Controller |
| eMMC Host Controller |
| GPIO |
| I2C Slave |
| I2C Slave To AHB Bridge |

- RISC-V solutions (TileLink + RISC-V CPU verification platform)

- Rapid turnaround on both creation and customization of Design and Verification IP to meet specific customer requirements

## Visit smartdv.com to view the full portfolio of IP solutions

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