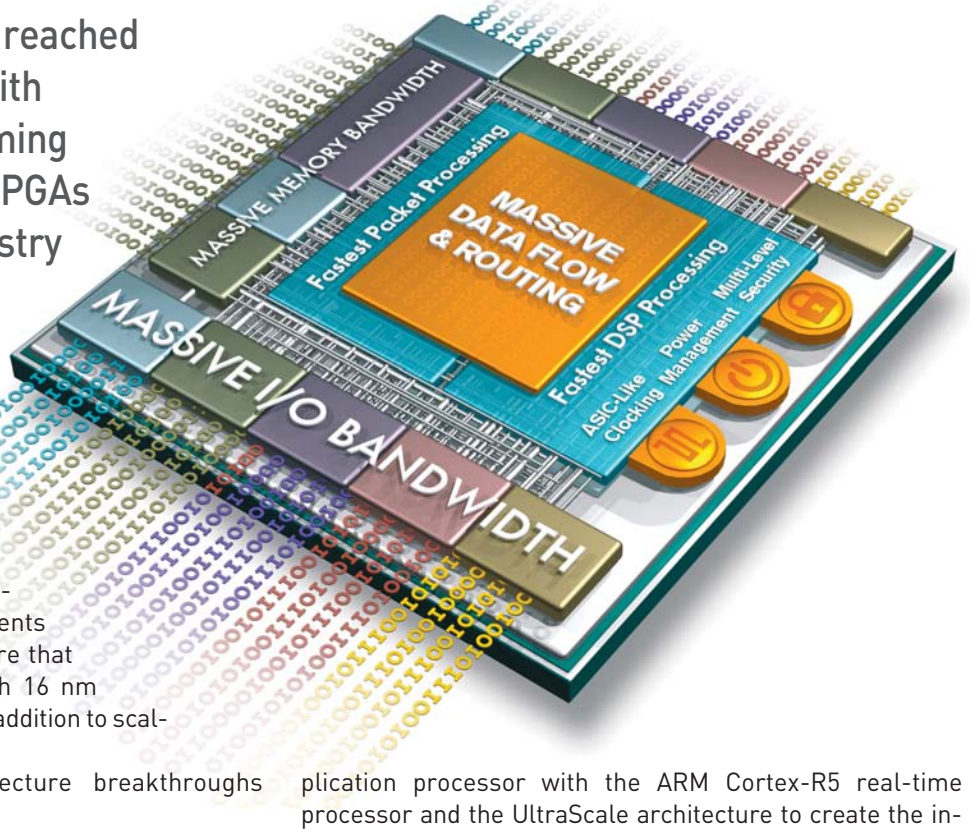
Current Generation of FPGAs Pose New Design and Verification Challenges

FPGA design sizes have reached unprecedented levels with million gate parts becoming increasingly common. FPGAs lead the rest of the industry in employing the most leading-edge fabrication technology.



UltraScale / UltraScale+

The UltraScale architecture is the industry's first application of leading-edge ASIC architectural enhancements in an all programmable architecture that scales from 20 nm planar through 16 nm FinFET technologies and beyond, in addition to scaling from monolithic through 3D ICs.

Some of the UltraScale architecture breakthroughs include:

- Strategic placement (virtually anywhere on the die) of ASIC-like system clocks.
- Latency-producing pipelining is virtually unnecessary in systems with massively parallel bus architecture, increasing system speed and capability.
- Potential timing-closure problems and interconnect bottlenecks are eliminated, even in systems requiring 90% or more resource utilization.
- 3D IC integration makes it possible to build larger devices one process generation ahead of the current industry standard.
- Increased system performance, including multi-gigabit serialtransceivers, I/O, and memory bandwidth is available within even smaller system power budgets.
- Greatly enhanced DSP and packet handling.

Zynq® UltraScale+ MPSoCs

Heterogeneous multiprocessor systems on-chip (MPSoC) are the next generation of multiprocessor architectures able to deal with the ever increasing performances and scalability demands. In fact, combining heterogeneous processors in the same architecture allows drawing on strength from each kind of processor, increasing overall system performance and efficiency.

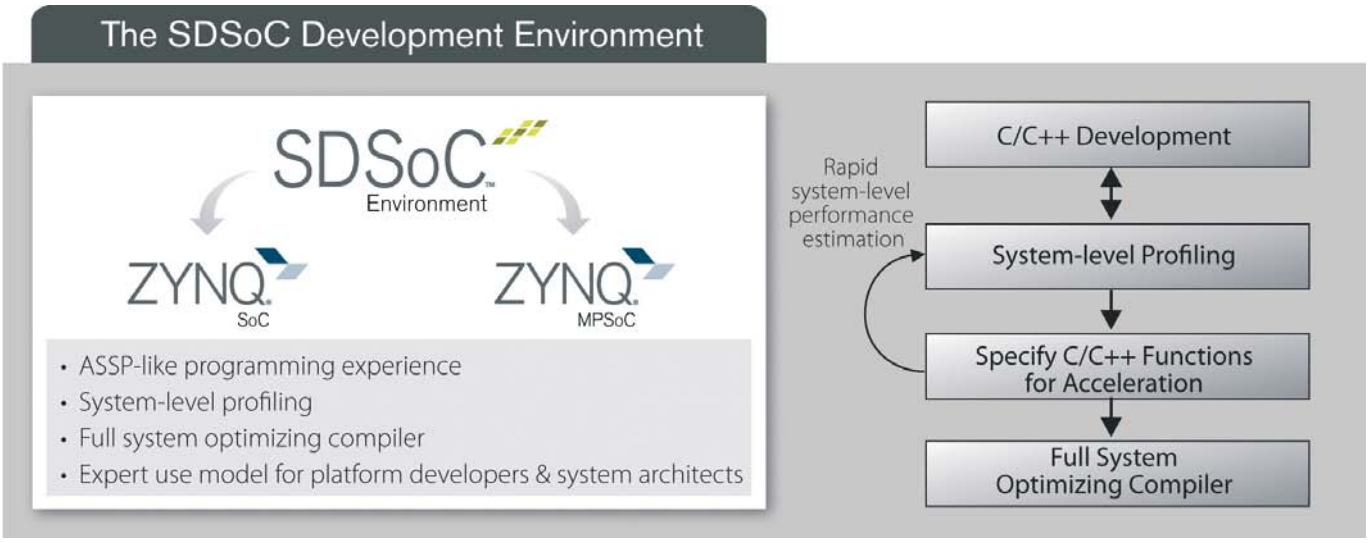
Zynq® UltraScale+ MPSoCs combine the ARM® v8-based Cortex®-A53 high-performance energy-efficient 64-bit application processor with the ARM Cortex-R5 real-time processor and the UltraScale architecture to create the industry's first all programmable MPSoCs. With next-generation programmable engines, security, safety, reliability, and scalability from 32 to 64 bits, the Zynq UltraScale+ MPSoCs provide power savings, processing, programmable acceleration, I/O, and memory bandwidth ideal for applications that require heterogeneous processing. In parallel with these advancements, as is the case with all innovative products, new challenges have emerged for the FPGA designer facing many different challenges while working on his or her project.

Power and Reliability Challenges

High-performance and low-power FPGAs require full custom design methodology, as well as power analysis tools for integration, modelling, power estimation and reliability.

Unlike ASICs, FPGA power consumption is highly design dependent because it is dictated by the utilization of logic resources, dedicated hardware and its routing to achieve the desired functionality.

Today, the I/O performance metric is not only dependent on the sample data rate (Gb/sec) but also on power consumption per unit data (mW/Gb). Because FPGAs typically are used in high data processing applications, Xilinx is constantly innovating through process technology, lower supply voltages, greater IP integration and various circuit design techniques to reduce power. But these advancements in high performance FPGAs impose significant challenges for power analysis solutions and methodologies.



Timing Closure Challenge

The timing closure problem for these high-end FPGAs has its root in the increased net delays in relation to the gate delays. The design size and interconnect issues together have led to an inefficient iterative methodology in completing designs.
Using the traditional FPGA design methodology, RTL is synthesized and sent through place and route. Timing is checked only at the end of the design flow. If the design fails to meet timing, modifications are made to the RTL and/or constraints and the flow is repeated. Modifications to the RTL can also have a global impact and lead the flow down a complete re-synthesis and a re-implementation. This iterative loop could sometimes take months to converge.

FPGA Verification

As devices grow and become more complex resembling complete systems, the task of verifying such a system becomes daunting.
Today's FPGAs are the size of ASICs from just a few years ago and the older techniques of only testing an FPGA in the lab are inadequate and irresponsible. Modern verification methodologies, like UVM (the SystemVerilog Universal Verification Methodology) or ABV (Assertion based Verification) are required to functionally verify modern FPGA designs.

New Design Challenges Demand New Design Methods

Traditional FPGA tools are very well suited for the majority of designers. For those complex designs targeting today's high-end FPGAs, however, new design tools will help achieve more aggressive design goals.
With Xilinx Vivado® Design Suite, some very unique and key technologies have become available to the FPGA community that could make timing closure a tractable problem. The solutions could broadly be classified under two categories: hierarchical design and silicon virtual prototyping. Hierarchical design tackles the design size and complexity issues. It enables incremental design, team-based design and an intellectual property (IP) reuse model. In contrast, silicon virtual prototyping allows for an early analysis of timing, utilization and congestion in the design to enable quicker and shorter iterations.
MPSoC application-specific platforms can be created with Xilinx's Vivado® Design Suite in combination with SDSoC. The platform creation also enables the ability to configure legacy RTL and IP to be leveraged as C-callable libraries.
The SDSoC development environment provides a C/C++ ASSP-like programming experience improving productivity for application development, system architecture definition and platform creation.
However, such a design introduces new challenges, especially for embedded software designers.

Introducing the Xilinx SDSoC Development Environment

The Zynq SoCs and MPSoCs are natural fit for design teams consisting of software and FPGA hardware engineers. Teams with limited or no hardware resources however have been challenged due to the RTL (VHDL or Verilog) development expertise needed to take full advantage of the benefit of the device.
To resolve this challenge and enable more design teams to take advantage of Zynq devices, Xilinx has introduced SDSoC™, a new C/C++ development environment.
The SDSoC Development Environment provides a greatly simplified ASSP-like C/C++ programming experience including an easy to use Eclipse integrated design environment (IDE) and a comprehensive development platform for heterogeneous Zynq platform deployment. Complete with the industry's first C/C++ full-system optimizing compiler, SDSoC delivers system level profiling, automated software acceleration in programmable logic, automated system connectivity generation, and libraries to speed programming. SDSoC enables the creation of complete heterogeneous multiprocessing systems, including software running on ARM/NEON processors, software accelerators in programmable logic and reuse of legacy HDL IP Blocks as C-callable libraries.

Knowledge Creates Performance

Well-trained engineers are the most valuable asset of a company. Competent switched first-hand knowledge is becoming increasingly important for the successful use of new technologies. Only well-trained R&D engineers can cope with the demands placed on it in the time allotted.
In order to face the challenges for modern FPGA design, ELECTRA IC and PLC2 partner to offer a broad portfolio of education services covering all aspects of FPGA design. The customer may choose from 80+ different workshops including advance FPGA architectures, VHDL, Verilog, SystemVerilog, High Level Synthesis, 'C/C++', SoC/MPSoC, SDSoC, Linux/Peta-Linux, Networking and Connectivity. All workshops might be customized for an in-house training to meet the special customer requirements.